



Docket No.: 394-1597

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :
Seiji SAWADA et al. :
Serial No. 08/246,582 : Group Art Unit: 2511
Filed: May 19, 1994 : Examiner: A. Zarabian
For: TEST CIRCUIT IN CLOCK SYNCHRONOUS SEMICONDUCTOR MEMORY
DEVICE

*5/Election
JL
11-18-94*

RESPONSE TO RESTRICTION REQUIREMENT

Honorable Commissioner of
Patents and Trademarks
Washington, D. C. 20231

NOV 14 1994

Sir:

Noting the Office Action of October 21, 1994 wherein
restriction has been required, Applicants hereby elect Group I
(claims 1-5 and 9-33) for prosecution in the above-identified
application.

Respectfully submitted,

LOWE, PRICE, LEBLANC & BECKER

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Date: November 9, 1994